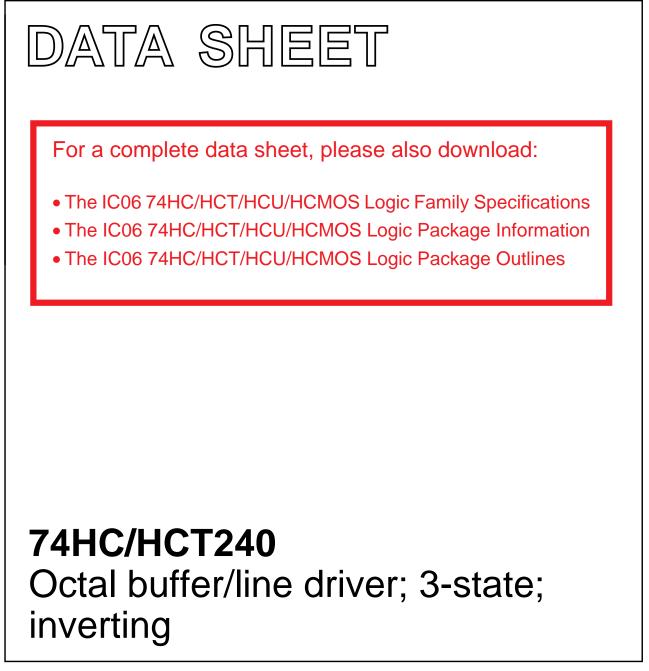
INTEGRATED CIRCUITS



Product specification File under Integrated Circuits, IC06 December 1990



74HC/HCT240

FEATURES

- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT240 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT240 are octal inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The "240" is identical to the "244" but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYP		
		CONDITIONS	НС	нст	
t _{PHL} / t _{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C _L = 15 pF; V _{CC} = 5 V	9	9	ns
CI	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

 $f_i = input frequency in MHz$

 $f_o = output frequency in MHz$

 $\Sigma (C_L \times V_{CC}^2 \times f_o) = sum of outputs$

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

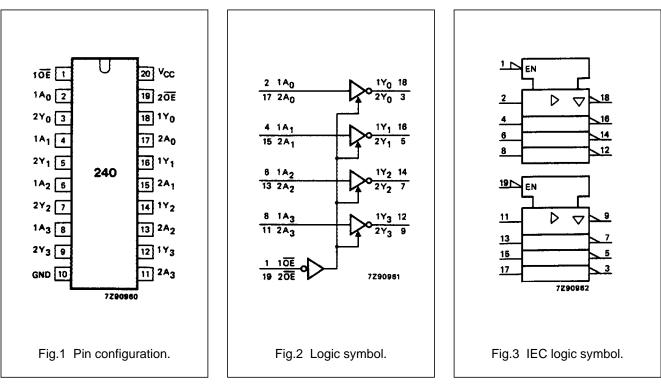
2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

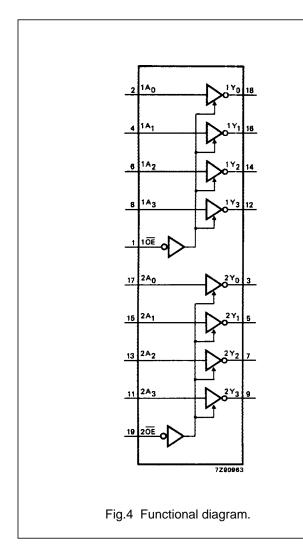
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	
1	1 0E	output enable input (active LOW)	
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs	
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs	
10	GND	ground (0 V)	
17, 15, 13, 11	2A ₀ to 2A ₃	data inputs	
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs	
19	2 0E	output enable input (active LOW)	
20	V _{CC}	positive supply voltage	



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FUNCTION TABLE

INP	OUTPUT				
nOE	nA _n	nY _n			
L	L	Н			
L	Н	L			
Н	X	Z			

Notes

- 1. H = HIGH voltage level
 - L = LOW voltage level

X = don't care

Z = high impedance OFF-state

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	PARAMETER	T _{amb} (°C)								TEST CONDITIONS	
SYMBOL		74HC									WAVEFORMS
		+25			-40 to +85		-40 to +125			V _{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay		30	100		125		150	ns	2.0	Fig.5
	1A _n to 1Y _n ;		11	20		25		30		4.5	
	2A _n to 2Y _n		9	17		21		26		6.0	
t _{PZH} / t _{PZL}	3-state output enable time		39	150		190		225	ns	2.0	Fig.6
	1 0E to 1Y _n ;		14	30		38		45		4.5	
	2 0E to 2Y _n		11	26		33		38		6.0	
t _{PHZ} / t _{PLZ}	3-state output disable time		41	150		190		225	ns	2.0	Fig.6
	$1\overline{OE}$ to $1Y_n$;		15	30		38		45		4.5	_
	$2\overline{OE}$ to $2Y_n$		12	26		33		38		6.0	
t _{THL} / t _{TLH}	output transition time		14	60		75		90	ns	2.0	Fig.5
			5	12		15		18		4.5	
			4	10		13		15		6.0	

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver II_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1A _n	1.50
2A _n 1OE	1.50
	0.70
2 0E	0.70

AC CHARACTERISTICS FOR 74HCT

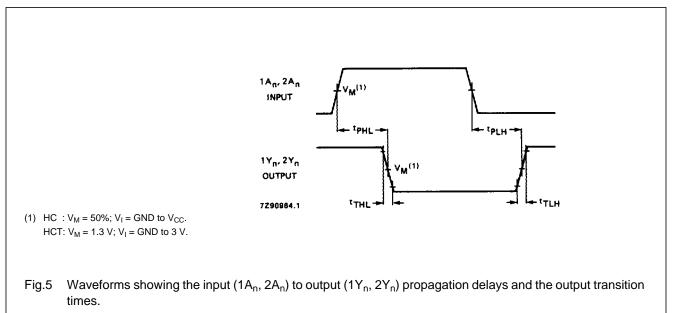
 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

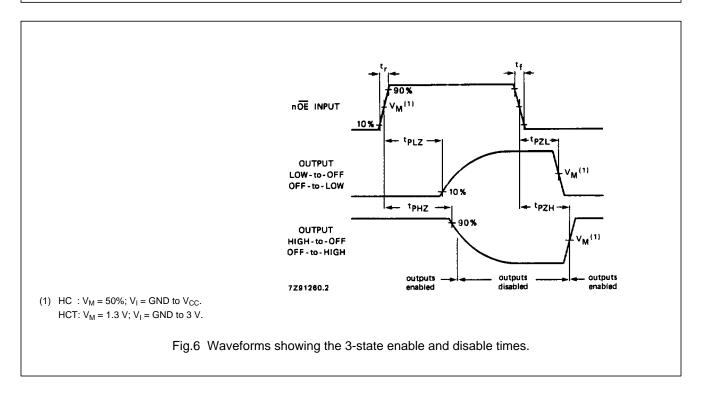
SYMBOL	PARAMETER	T _{amb} (°C)								TEST CONDITIONS	
		74HCT									WAVEFORMS
		+25			-40 to +85		-40 to +125			V _{CC} (V)	WAVEFORMIS
		min.	typ.	max.	min.	max.	min.	max.		(.,	
t _{PHL} / t _{PLH}	propagation delay 1A _n to 1Y _n ; 2A _n to 2Y _n		11	20		25		30	ns	4.5	Fig.5
t _{PZH} / t _{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$		13	30		38		45	ns	4.5	Fig.6
t _{PHZ} / t _{PLZ}	$\begin{array}{l} \mbox{3-state output disable time} \\ 1 \overline{OE} \mbox{ to } 1Y_n; \\ 2 \overline{OE} \mbox{ to } 2Y_n \end{array}$		13	25		31		38	ns	4.5	Fig.6
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.5

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Product specification

AC WAVEFORMS





PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".